IN THE CLAIMS:

Please cancel claim 2, and amend the claims as follows:

1. (Currently Amended) A method for determining a repair solution for a memory module in a test system, comprising:

determining, for each memory area of the memory module, a defect datum;

generating defect addresses for all defective memory areas;

storing the defect addresses in the test system; and

selecting one or more replacement redundant groups based on the defect addresses stored in the test system, wherein each memory area is addressable via a word line group comprising one or more word lines or via a bit line group comprising one or more bit lines, and wherein the one or more replacement redundant groups are selected from a redundant word line group if the defective memory areas that are addressable by a common word line group exceeds a first maximum number and from a redundant bit line group if the defective memory areas that are addressable by a common bit line group exceeds a second maximum number, wherein the first maximum number and the second maximum number are greater than zero.

2. (Canceled) The method of claim 1, wherein each memory area is addressable via a word line group comprising one or more word lines or via a bit line group comprising one or more bit lines; and wherein the one or more replacement redundant groups are selected from a redundant word line group if the defective memory areas that are addressable by a common word line group exceeds a first maximum number and from a redundant bit line group if the defective memory areas that are addressable by a common bit line group exceeds a second maximum number.

3. (Original) The method of claim 2, wherein the one or more replacement redundant groups are selected for all remaining defective memory areas that were not replaced by one of the redundant word line group and the redundant bit line group.

4. (Original) The method of claim 2, wherein the first maximum number corresponds to available redundant bit line groups and the second maximum number corresponds to available redundant word line groups.

5. (Original) The method of claim 1, wherein defect addresses are stored in a memory unit which includes a first memory segment having a first number of defect address memory locations for storing defect addresses in a word line group and a second memory segment having a second number of defect address memory locations for storing defect addresses in a bit line group.

6. (Original) The method of claim 5, wherein each memory segment includes a replacement register for indicating an overflow condition of the memory segment, and wherein the evaluation unit unconditionally defines a redundant word line group as repair solution for the defective memory areas which can be addressed via a word line group if the replacement register for the first memory segment indicates an overflow condition, and unconditionally defining a redundant bit line group as repair solution for the defective memory areas which can be addressed via a bit line group, if the replacement register for the second memory segment indicates an overflow condition.

7. (Currently Amended) A test device for determining a repair solution for a memory module, comprising:

a control unit for carrying out a test operation for memory areas in the memory module and determining defective memory areas;

a memory unit for storing defect addresses of defective memory areas;

a converter circuit for converting defect data corresponding to defect memory areas into defect addresses for storing in the memory unit; and

an evaluation unit for selecting one or more replacement redundant groups based on the stored defect addresses, wherein each memory area is addressable via a word line group comprising one or more word lines or via a bit line group comprising one or more bit lines, and wherein the one or more replacement redundant groups are selected from a redundant word line group if the defective memory areas that are

addressable by a common word line group exceeds a first maximum number and from a redundant bit line group if the defective memory areas that are addressable by a common bit line group exceeds a second maximum number, wherein the first maximum number and the second maximum number are greater than zero.

8. (Original) The test device of claim 7, wherein the evaluation unit selects the one or more replacement redundant groups from one or more redundant word line groups and one or more redundant bit line groups.

9. (Original) The test device of claim 8, wherein the memory unit includes a first memory segment having a first number of defect address memory locations for storing defect addresses in a word line group and a second memory segment having a second number of defect address memory locations for storing defect addresses in a bit line group.

10. (Original) The test device of claim 9, wherein the first number corresponds to available redundant bit line groups on the memory module and the second number corresponds to available redundant word line groups on the memory module.

11. (Original) The test device of claim 9, wherein each memory segment includes a replacement register for indicating an overflow condition of the memory segment.

12. (Original) The test device of claim 11, wherein the evaluation unit unconditionally defines a redundant word line group as repair solution for the defective memory areas which can be addressed via a word line group if the replacement register for the first memory segment indicates an overflow condition, and unconditionally defining a redundant bit line group as repair solution for the defective memory areas which can be addressed via a bit line group, if the replacement register for the second memory segment indicates an overflow condition.

13. (Original) The test device of claim 12, wherein the evaluation unit selects the one or more replacement redundant groups for all remaining defective memory areas that were not replaced by one of the redundant word line group and the redundant bit line group.

14. (Original) The test device of claim 7, further comprising:

a comparator circuit for comparing written data and read-out data to generate defect data.

15. (Currently Amended) A test system, comprising:

a connectable memory module; and

a test device, connectable to the memory module, for determining a repair solution for the memory module, the test device comprising a control unit for carrying out a test operation for memory areas in the memory module and determining defective memory areas, a memory unit for storing defect addresses of defective memory areas, and an evaluation unit for selecting one or more replacement redundant groups based on the stored defect addresses, wherein each memory area is addressable via a word line group comprising one or more word lines or via a bit line group comprising one or more bit lines, and wherein the one or more replacement redundant groups are selected from a redundant word line group if the defective memory areas that are addressable by a common word line group exceeds a first maximum number and from a redundant bit line group if the defective memory areas that are addressable by a common bit line group exceeds a second maximum number, wherein the first maximum number and the second maximum number are greater than zero.

16. (Original) The test system of claim 15, wherein the memory module includes a comparator circuit for comparing written data and read-out data to generate defect data.

17. (Original) The test system of claim 15, wherein the test device further comprises a comparator circuit for comparing written data and read-out data to generate defect data.

18. (Currently Amended) A method for determining a repair solution for a memory module in a test system, comprising:

generating defect addresses corresponding to all defective memory areas of the memory areas of the memory module;

storing the defect addresses in a memory unit in the test system, wherein the memory unit includes a first memory segment having a first number of defect address memory locations for storing defect addresses in a word line group and a second memory segment having a second number of defect address memory locations for storing defect addresses in a bit line group; and

selecting one or more replacement redundant groups based on the defect addresses stored in the memory unit, wherein the evaluation unit selects the one or more replacement redundant groups from one or more redundant word line groups and one or more redundant bit line groups, wherein each memory area is addressable via a word line group comprising one or more word lines or via a bit line group comprising one or more bit lines, and wherein the one or more replacement redundant groups are selected from a redundant word line group if the defective memory areas that are addressable by a common word line group exceeds a first maximum number and from a redundant bit line group if the defective memory areas that are addressable by a common bit line group exceeds a second maximum number, wherein the first maximum number and the second maximum number are greater than zero.[[.]]

19. (Original) The method of claim 18, wherein the first number corresponds to available redundant bit line groups on the memory module and the second number corresponds to available redundant word line groups on the memory module.

20. (Original) The method of claim 18, wherein each memory segment includes a replacement register for indicating an overflow condition of the memory segment, and

wherein the evaluation unit unconditionally defines a redundant word line group as repair solution for the defective memory areas which can be addressed via a word line group if the replacement register for the first memory segment indicates an overflow condition, and unconditionally defining a redundant bit line group as repair solution for the defective memory areas which can be addressed via a bit line group, if the replacement register for the second memory segment indicates an overflow condition.

21. (Original) The method of claim 18, wherein the one or more replacement redundant groups are selected for all remaining defective memory areas that were not replaced by one of the redundant word line group and the redundant bit line group.